KEYED AUTOMATIC GAIN CONTROL CIRCUIT FOR TV RECEIVERS

By Samuel A. Schwartz

I. INTRODUCTION

The performance of a television receiver throughout a wide range of input signal levels is largely a result of both its gain control characteristics and automatic-gain-control system. The gain-controlled portions of conventional television [illegible] fier. Some of the lower cost receivers have a total of two i-f stages and gain control is applied to the first stage only.

Various types of agc systems have been used in television receivers and the most commonly employed types include peak agc, average agc, and gated amplified agc. The latter type is commonly referred to as keyed agc and has several important advantages over the other types. Therefore, all further explanation in this paper will be restricted to keyed agc. These advantages are as follows:

1. It has a large agc figure of merit due to the high loop gain of the keyed agc system.
2. The sampling process of the keyed agc system results in a short time constant and resulting fast control action. This feature reduces the effect of rapid signal fluctuations produced by airplane reflections.
3. Good noise immunity is achieved by the sampling process that "looks" at the highest video level or sync tips, where the signal-to-noise ratio is the highest. Large amplitude impulse noise pulses occurring other than in the sync interval have no effect on agc.

II. DESIGN OF AGC

The agc circuit as shown in Fig. 1 consists of a keyer stage that produces the agc voltage and an amplifier-inverter stage for processing the agc voltage. The latter is necessitated by the required polarity inversion of the agc voltage for use with the forward agc control mode and also by the agc power requirements for the r-f and i-f stages.

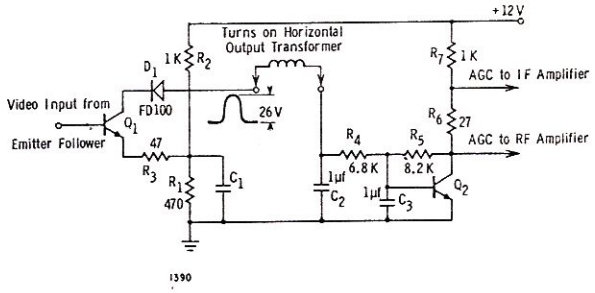

FIG. 1. Schematic diagram of keyer and amplifier inverter.

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In addition to the above functions, the amplifier-inverter supplies the correct maximum gain bias for the i-f stages as well as providing the correct delay voltage for the r-f stage. Thus, the design of the keyer is simplified in that it needs to supply an agc voltage that goes only from zero to a convenient maximum value which is then scaled, offset, and delayed in the amplifier-inverter stage.

The keyer is similar to a Class-C amplifier in that the input signal drives the stage on from a cutoff condition. However, collector voltage for the stage is not continuous but is supplied in pulses coincident with the horizontal sync pulses. These pulses are obtained from a separate winding of the horizontal output transformer. A diode in the collector circuit of the keyer prevents the agc voltage from forward biasing the collector-base diode of the keyer transistor during the time interval between keying pulses.

The transistors used in both the keyer stage and the inverter are general purpose types designated the SE1002. The keyer stage, besides developing the agc voltage, amplifies the agc voltage, and also provides the agc reference threshold level. The level detecting is accomplished by the base-emitter diode of the keyer transistor. The emitter is biased to the absolute voltage level corresponding to the minimum value of the range of video voltage entering the agc circuitry as shown in Fig. 2.

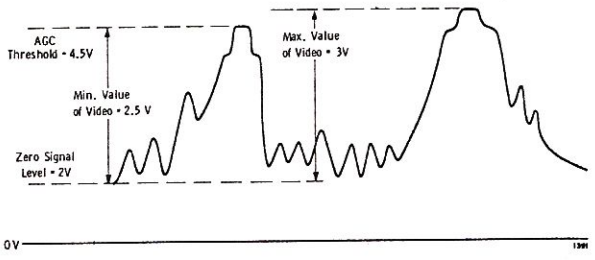

FIG. 2. Video voltage levels at keyer.

Thus the emitter voltage is as follows:

$$V_E = E_c - V_{be} = 4.5 - 0.7 = 3.8 \text{ volts}$$

Since the keyer works directly from an emitter follower output at which point the limits of video excursion have been defined above, it is not necessary to include the second detector loss and, therefore, $\beta(0) = 1$. The required loop gain within the agc circuitry for d-c control is (Ref. 1)

$$A_1(0)\,\beta(0) = \frac{e_c(\max)}{e_o(\max) - e_o(\min)}$$

$$A_1(0) = \frac{e_c(\max)}{e_o(\max) - e_o(\min)}$$

At the limiting condition of maximum video output of 3 V, the required agc voltage for the i-f amplifier is 5.4 volts. Assuming that the scaling factor or gain of the amplifier-inverter is equal to -1, the maximum value of agc voltage to be developed by the keyer is -5.4 volts. From the requirements for the video and sync takeoffs, it would be desirable to hold the detected output video level within the range of 2.5 to 3 volts from agc threshold to maximum signal input as shown in Fig. 2.

The required gain in the keyer stage is, then, as follows:

$$A_1(0) = 5.4/(3 - 2.5) = 10.8$$

The gain of the keyer in terms of circuit values is

$$A_1(0) = \frac{t_s}{t_h} \times \frac{R_L}{R_E}$$

A typical example in calculating the value of R_E is as follows (see Appendix Eq. (9)):

$$R_E = \frac{t_s}{t_h} \times \frac{R_L}{A_1}$$

where

t_s = 4.7 μsec (horizontal sync pulse)

t_h = 63.5 μsec (period of one line)

R_L = 6.8 K (This value is chosen to be compatible with time constant requirements as well as other circuit values in the amplifier-inverter.)

which gives

$$R_E = \left(\frac{4.7 \times 10^{-6}}{63.5 \times 10^{-6}}\right)\left(\frac{6.8 \times 10^{3}}{10.8}\right)$$

$$= 46.5\ \Omega$$

The average transistor current and thus the current through the reference or threshold bias source is

$$i_c(\text{avg}) = \left(\frac{E_S - E_R}{R_E}\right)\left(\frac{t_s}{t_h}\right)$$

$$= \left(\frac{3 - 2.5}{46.5}\right)\left(\frac{4.7 \times 10^{-6}}{63.5 \times 10^{-6}}\right) = 0.8 \text{ ma}$$

The regulation of the bias network can be made adequate by allowing the current through the network to be equal to 10 i_c(avg) as shown in Fig. 3.

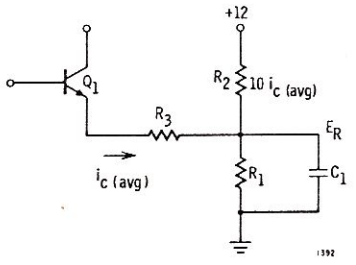

FIG. 3. Circuit of bias network.

$$R_1 = E_R/[i_c(\text{avg})\ (10 + 1)]$$

$$= 3.8/[(0.8 \times 10^{-3})\ (11)] = 432\ \Omega$$

$$R_2 = [12 - E_R]/[10\ i_c(\text{avg})]$$

$$= [12 - 3.8]/[(0.8 \times 10^{-3})\ (10)] = 1020\ \Omega$$

Resistor R_1 is bypassed by capacitor C_1 to prevent degeneration during the conducting interval t_s.

The value of the capacitor C_2 is chosen to be consistent with the requirements for adequate speed of response of the agc circuit. The time constant of C_2 and R_4 is approximately equal to 100 horizontal line periods.

$$R_4 C_2 = (100)\ (63.5 \times 10^{-6})\ \text{sec}$$

$$C_2 = \frac{(100)\ (63.5 \times 10^{-6})}{6.8 \times 10^{3}} = 0.93\ \mu\text{f}$$

It should be noted that the filter in the agc circuit described here places the filter at the output of the agc voltage amplifier (keyer stage), whereas the analysis in Appendix I shows the filter at the input to the amplifier. The difference lies in the fact that the general case of feedback amplifier analyzed in the Appendix does not involve sampling of the controlled signal. In the sampling case the filter follows the sampling process to provide "memory" or storage of the agc voltage between samples. Thus the problem of modulation filtering does not exist in the sampled case because the modulation that could possibly be objectionable occurs during the sampler off time intervals.

The loop gain AB is modified by the low-pass filter response in either case and the resulting loop gain AB (ω) contains only a single pole at $-1/(R_4 C_2)$ and thus the loop is stable for all values of AB

The collector driving pulse for the keyer stage has an amplitude of 20 volts. Although the value is not critical, it must be slightly greater than the sum of the maximum value of agc voltage, the reference voltage, the diode D_1 drop, and the drop across transistor Q_1 in a nonsaturated condition.

The amplifier-inverter as shown in Fig. 1 is designed to have a gain of -1 by proper choice of feedback resistor R_5. The value of the collector load, comprised of resistors R_6 and R_7, is selected to set operation close to maximum beta of the transistor as well as being able to supply approximately 6 ma of base current to the gain-controlled carrier amplifiers. A suitable value for R_1 is 1 kilohm. The value of R_4, the keyer load resistor that also serves as an input resistor for the amplifier-inverter, is 6.8 kilohms. Assuming an average beta of 40, the value of feedback resistor R_5 is as follows:

$$R_5 = \frac{(R_6 + R_7)\, R_4\, (\beta + 1)}{\beta\, (R_6 + R_7) - R_4} \quad \text{(See Appendix III)}$$

$$= \frac{(1 \times 10^3)\,(6.8 \times 10^3)\,(40 + 1)}{40\,(1 \times 10^3) - (6.8 \times 10^3)} = 8.4\ \text{K}\Omega$$

The collector load of Q_2 is tapped so that the correct agc offset voltage is available for the i-f amplifier under the condition of maximum gain when no agc voltage is developed by the keyer stage. The d-c offset voltage at the collector is represented by the following equation (see Appendix Eq. 16A):

$$e_0 = V_{CC}\left[\frac{R_5}{R_5 + R_L\,(\beta+1)}\right] + V_{be}\left[\frac{\beta R_L R_5 + R_L R_4\,(\beta + 1)}{R_4 R_5 + R_L R_4\,(\beta + 1)}\right]$$

Substituting these values

$V_{CC} = 12$ V, $R_5 = 8.4$ KΩ, $R_L = R_5 + R_6 = 1$ KΩ, $R_4 = 6.8$ KΩ, $\beta = 40$, $V_{be} = 0.7$ V

gives

$$E_0 = 12\,\frac{8.4 \times 10^3}{8.4 \times 10^3 + 10^3\,(40 + 1)} + 0.7\,\frac{40(10^3)(8.4\times10^3) + (10^3)(6.8\times10^3)(40+1)}{(6.8\times10^3)(8.4\times10^3) + (10^3)(6.8\times10^3)(40+1)}$$

$$= 2.04 + 1.28 = 3.32 \text{ volts}$$

The desired agc voltage range for the i-f amplifier is 3.5 to 8.9 volts so that it becomes necessary to make the voltage at the junction of R_6 and R_7 equal to 3.5 when the collector voltage is 3.32 volts. The values of resistors R_6 and R_7

$$R_6 = R_L\left(\frac{V_{if} - e_0}{V_{CC} - e_0}\right)$$

$$R_7 = R_L\left(1 - \frac{V_{if} - e_0}{V_{CC} - e_0}\right)$$

Using the values previously given for V_{if}, e_0, and V_{CC}, the resistances are as follows:

$$R_6 = 10^3\left(\frac{3.5 - 3.32}{12 - 3.32}\right) = 27.5\ \Omega$$

$$R_7 = 10^3\left(1 - \frac{3.5 - 3.32}{12 - 3.32}\right) = 972.5\ \Omega$$

As a practical matter, the output of the amplifier-inverter will vary somewhat with beta and resistor tolerances so that the desired output from the junction of R_6 and R_7 could be equal to the output voltage directly at the collector. This has a minor effect on the over-all gain controlled amplifier as the plot of gain versus voltage has a rather flat maxima as is typified in Fig. 4. Thus, the i-f agc voltage may be taken directly from the collector of the amplifier inverter.

It is advantageous to delay the application of agc voltage to the r-f amplifier until the i-f amplifier gain has been reduced approximately 20 db from the maximum gain value. This delay in agc voltage can be accomplished by a voltage limiter circuit utilizing a diode. In the case where the r-f amplifier uses the forward agc mode, the delay may be designed into the tuner. This is accomplished by allowing the lowest value of agc voltage to slightly reverse bias the r-f amplifier from the maximum gain point as seen in Fig. 4.

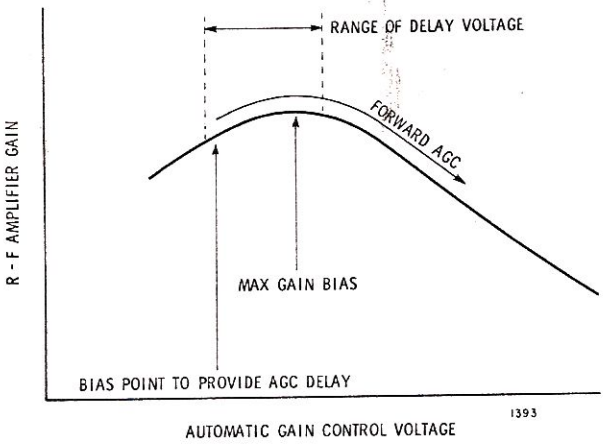

FIG. 4. R-f amplifier gain characteristic.

The capacitor C_3 was placed in the circuit as a practical expedient after the television receiver containing the above described keyed agc circuit was completed. It was found that the "fields" were pairing and consequently proper interlace could not be obtained. The trouble was traced to the agc circuit which was "picking" up horizontal pulses from the horizontal sweep circuit and reproducing the pulses in the output agc voltage. Consequently, the video carrier signal was being modulated by the agc voltage with the result that the received sync information was distorted. This produced an effect such that the output of the vertical integrator was different on alternate fields. The difference was equivalent to a time interval equal to one-half the horizontal sweep period. Thus, alternate fields were caused to coincide, producing pairing. The capacitor produces no additional phase shifting in the circuit because it is placed at the null point of the amplifier-inverter which is in essence an operational amplifier.

III. PERFORMANCE TEST

The performance criterion of the amplifier can be specified by the agc Figure of Merit as defined below (Ref. 2).

$$F_{agc} = 20 \log E_1 / E_2$$

where

E_1 = r-f input of 0.1 volt

E_2 = r-f input required to produce an output signal 10 db below that produced by E_1.

The values E_1 and E_2 can be obtained from direct measurements on the equipment or can be taken from an agc regulation characteristic such as shown in Fig. 5. The curve can be obtained from measured data or it can be calculated point by

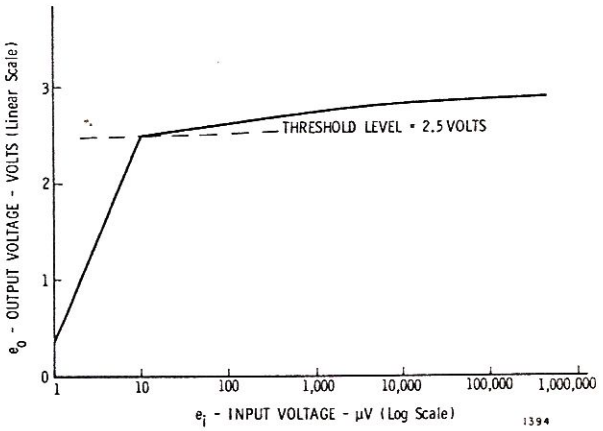

FIG. 5. Regulation characteristic of agc.

point if the amplifier's gain-control characteristic is known. A typical characteristic for forward agc control is shown in Fig. 6.

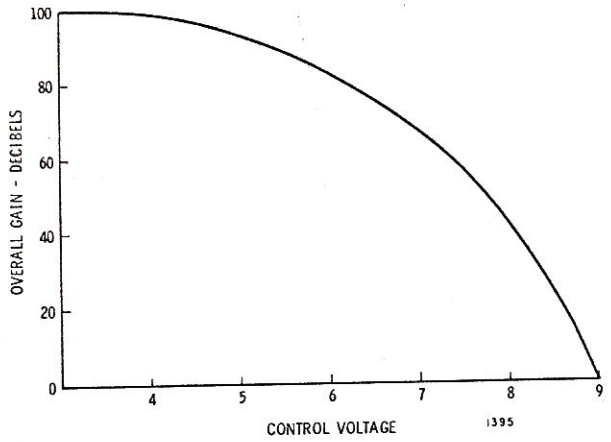

FIG. 6. Amplifier control characteristics.

The procedure for obtaining the regulation characteristic from the amplifier control characteristic is as follows:

1. Select an arbitrary output voltage, e_0, from the second detector.
2. If e_0 is larger than the agc threshold voltage, multiply the difference between the two voltages by the $A(0)\beta(0)$ of the keyer stage and arrive at the agc voltage, e_c. If e_0 is smaller than the agc threshold voltage, e_c will be equal to zero.
3. The value of e_c placed on the gain control characteristic will yield a gain figure $M(e_c)$.
4. The input voltage e_i corresponding to e_0 will be $e_0 / M(e_c)$.
5. Plot various values of e_0 versus e_i to obtain the agc regulation characteristic.

IV. APPENDIX I

An agc circuit in combination with gain controlled r-f and i-f amplifiers is essentially a form of feedback amplifier. (Ref. 1)

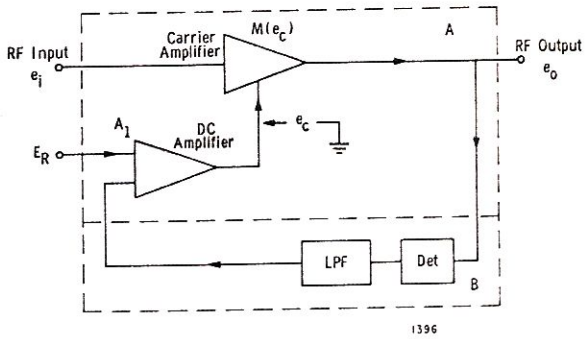

FIG. 1A. Block diagram of feedback amplifier.

Using conventional feedback theory, the feedback amplifier consists of a forward transmission circuit, A; a reverse transmission circuit, β; and a comparison circuit that adds the signal from β to an external reference signal, E_R, resulting in a signal that controls the output of A.

The block diagram shown in Fig. 1A shows the feedback amplifier composed of the pertinent components of the television receiver. The gain controlled r-f and i-f amplifiers have been lumped into a carrier amplifier that modulates the r-f input signal, e_i, as a function of the controlling voltage, e_c. This voltage is obtained as a result of comparing the feedback signal with the reference signal and amplification of the resulting difference signal. Thus the forward transmission circuit, A, includes the envelope gain $M(e_c)$ of the carrier amplifier and the gain A_1 of the d-c amplifier.

Since the primary purpose of the agc is to control output level of a carrier signal, a detector must be used to provide a feedback voltage proportional to carrier level. The reverse transmission path, β, thus contains the second detector and an accompanying low pass filter (LPF).

Refer to Fig.1A and consider all r-f voltages as envelope or peak level values. Then the response of the forward transmission is as follows:

$$\begin{aligned} e_0 &= [A_1 M(e_c)][E_R + B e_0] \\ &= A(E_R + B e_0) \\ &= E_R A/(1 - AB) \end{aligned} \tag{1}$$

For the case where: $|AB| \gg 1$,

$$e_0 \simeq -E_R/B \tag{2}$$

Thus it may be observed that the output level is independent of total loop gain A that includes the forward transmission gain, $M(e_c)$, and the variations in input voltage, e_i, as long as $|A\beta| \gg 1$. The effectiveness of the feedback system in suppressing the effects of gain variations may be obtained by differentiating (1) with respect to A and dividing the result by (1).

$$de_0 = \frac{dA}{(1 - AB)^2} E_R \tag{3}$$

$$\frac{de_0}{e_0} = \left(\frac{1}{1 - AB}\right)\left(\frac{dA}{A}\right) \tag{4}$$

If A is replaced by A_1 and $M(e_c)$ and noting that only $M(e_c)$ can change to accommodate changes in input level e_i, the following results:

$$\begin{aligned} \frac{de_0}{e_0} &= \left\{\frac{1}{1 - AB}\right\}\left\{\frac{d[A_1 M(e_c)]}{A_1 M(e_c)}\right\} \\ &= \left[\frac{1}{1 - AB}\right]\left[\frac{A_1 dM(e_c)}{A_1 M(e_c)}\right] \\ &= \left[\frac{1}{1 - AB}\right]\left[\frac{dM(e_c)}{M(e_c)}\right] \end{aligned} \tag{5}$$

Therefore, changes in gain of the carrier amplifier, corresponding to changes in input level, are reduced by the factor $(1 - A\beta)$ in affecting a change in output voltage.

As the value $M(e_c)$ must change inversely to changes in e_i in order to hold e_0 constant, the percentage change in the quantities must be equal as follows:

$$\frac{de_i}{e_i} = \frac{dM(e_c)}{M(e_c)} \tag{6}$$

Substitution of Eq. (6) in Eq. (5) yields:

$$\frac{de_0}{e_0} = \left(\frac{1}{1 - AB}\right)\left(\frac{de_i}{e_i}\right)$$

$$\frac{(de_0)/e_0}{(de_i)/e_i} = \frac{1}{1 - AB} \tag{7}$$

Equation (7) shows that the percentage change in output voltage is smaller than the percentage change in input voltage by the factor $1 - AB$.

It is obvious from Eq. (2) that modulation components of e_0 would also be suppressed were it not for the low-pass filter following the second detector. This filter causes AB to be less than unity over the range of desired modulation frequencies and thus the output e_0 is not held constant but is allowed to reproduce the modulation components.

V. APPENDIX II

The equivalent circuit of the keyer stage is shown in Fig. 2A.

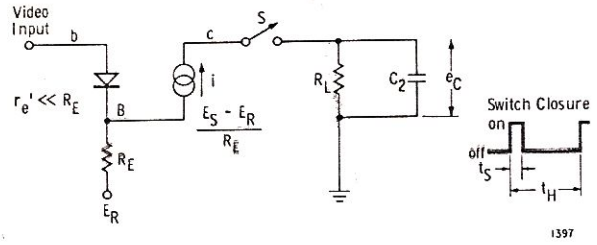

FIG. 2A. Equivalent circuit of keyer.

The keyer is actuated by a horizontal keying pulse that is coincident with the horizontal sync voltage, E_S, and has the effect of closing the switch S in Fig. 2A for the effective duration t_s of the horizontal sync pulse. The pulses of collector current are integrated to produce an average output voltage e_c by the action of R_L and C_2.

$$e_c(0) = i \frac{t_s}{t_h} R_L$$

$$= \left(\frac{E_S - E_R}{R_E}\right)\left(\frac{t_s}{t_h} R_L\right) \qquad (8)$$

The d-c gain of the keyer is

$$A_1(0) = \frac{e_c(0)}{E_S - E_R}$$

$$= \frac{(E_S - E_R)/R_E \left[(t_s/t_h) R_L\right]}{E_S - E_R}$$

$$= \left(\frac{t_s}{t_h}\right)\left(\frac{R_L}{R_E}\right) \qquad (9)$$

and the average current through the transistor is

$$i_c(\text{avg}) = \left(\frac{E_S - E_R}{R_E}\right)\left(\frac{t_s}{t_h}\right)$$

VI. APPENDIX III

The amplifier inverter is shown in Fig. 3A and is analyzed as a d-c amplifier.

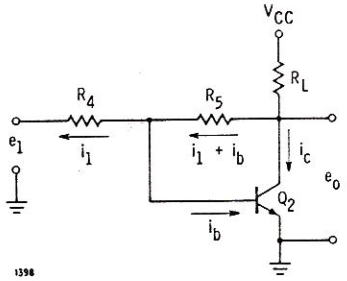

FIG. 3A. Schematic diagram of amplifier inverter.

The output voltage, e_0, which is the desired agc voltage is expressed as follows:

$$e_0 = V_{CC} - R_L (i_c + i_b + i_1) \qquad (10)$$

$$i_1 + i_b = (e_0 - V_{be})/R_5 \qquad (11)$$

$$i_1 = (V_{be} - e_1)/R_4 \qquad (12)$$

$$i_b = \left[(e_0 - V_{be})/R_5\right] - i_1$$
$$= \left[(e_0 - V_{be})/R_5\right] - \left[(V_{be} - e_1)/R_4\right] \qquad (13)$$

$$i_c = \beta_0 i_b \qquad (14)$$

Substitution of Eqs. (11), (13), and (14) in Eq. (10) gives

$$e_0 = V_{CC} - R_L\left[\beta_0\left(\frac{e_0 - V_{be}}{R_5} - \frac{V_{be} - e_1}{R_4}\right) + \frac{e_0 - V_{be}}{R_5}\right] \qquad (15)$$

Equation (15) can be reduced to the following:

$$e_0 = V_{CC}\left[\frac{R_5}{R_5 + R_L(\beta_0 + 1)}\right] + V_{be}\left[\frac{\beta_0 R_L R_5 + R_L R_4(\beta_0 + 1)}{R_4 R_5 + R_L R_4(\beta_0 + 1)}\right] - e_1\left[\frac{\beta_0 R_L R_5}{R_4 R_5 + R_L R_4(\beta_0 + 1)}\right] \quad (16)$$

The first term in Eq. (16) represents the d-c offset voltage at the collector due to the base bias being derived from the collector voltage. The second term is the d-c offset voltage due to the effect of the base-emitter voltage V_{be}. The third term represents the component of output voltage due to the input voltage e_1. Thus, the voltage gain of the amplifier can be derived using the last term as follows:

$$e_0 = -e_1\left[\frac{\beta_0 R_L R_5}{R_4 R_5 + R_L R_4(\beta_0 + 1)}\right] \quad (17)$$

$$\frac{e_0}{e_1} = -\frac{\beta_0 R_L R_5}{R_4 R_5 + R_L R_4(\beta_0 + 1)} \quad (18)$$

In order to satisfy the required amplifier voltage gain of unity, Eq. (18) is set equal to unity and a solution for the feedback resistor R_5 in terms of the other circuit values is:

$$\frac{\beta_0 R_L R_5}{R_4 R_5 + R_L R_4(\beta_0 + 1)} = 1 \quad (19)$$

$$R_5 = \frac{R_L R_4(\beta_0 + 1)}{\beta_0 R_L - R_4} \quad (20)$$

The collector load resistance R_L is replaced by resistors R_6 and R_7 in order to supply the low limit values of age, so that Eq. (20) becomes

$$R_5 = \frac{(R_6 + R_7)(R_4)(\beta_0 + 1)}{\beta_0(R_6 + R_7) - R_4}$$

The voltage at the tap of R_6 and R_7, as shown in Fig. 1 is calculated as follows:

$$V_{if} = e_0 + \frac{R_6}{R_6 + R_7}(V_{CC} - e_0) \quad (21)$$

$$R_6 + R_7 = R_L \quad (22)$$

Substitution of Eq. (22) in Eq. (21) yields the following:

$$R_7 = R_L\left(1 - \frac{V_{if} - e_0}{V_{CC} - e_0}\right) \quad (23)$$

$$R_6 = R_L\left(\frac{V_{if} - e_0}{V_{CC} - e_0}\right) \quad (24)$$

CONCLUSION

This agc circuit design is not critical in its components and the general-purpose silicon transistors used gave more than satisfactory performance. Also the circuit is extremely simple and utilizes the fewest number of components. The agc of the transistorized TV receiver in which the circuit was employed has proved to be equal to that of the best keyed agc vacuum tube sets. It was shown that two transistors are required to control both the r-f and i-f amplifiers with forward biased agc. As both the keyer and inverter stages operate at low collector currents, heating is not a problem and reliability is enhanced.

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LIST OF SYMBOLS

A_1	Voltage gain of keyer stage or agc control voltage amplifier
$A_1(0)$	D-C gain of keyer stage or agc control voltage amplifier
A_V	Voltage amplification
β	Transmission factor of feedback circuit
$\beta(0)$	D-C transmission factor of feedback circuit
C'_{be}	Diffusion capacitance
E_c	AGC control voltage threshold
e_c	AGC control voltage
$e_c(max)$	Maximum required value of agc control voltage
e_i	R-F input voltage
e_0	Envelope value of r-f amplifier output; also used for second detector output
$e_0(max)$	Maximum desired value of e_0
$e_0(min)$	Minimum desired value of e_0
E_R	Voltage of reference or agc threshold
E_S	Voltage level of horizontal sync pulse
F_{agc}	AGC figure of merit
$i_c(avg)$	Average current through keyer transistor
$M(e_c)$	Envelope gain of carrier amplifier controlled by voltage e_c
r'_b	Intrinsic base resistance
r'_e	Intrinsic emitter resistance
R_E	Resistance in emitter circuit
R_L	Collector load resistor
t_h	Period of horizontal sweep and retrace interval
t_s	Period of horizontal sync pulse
V_{be}	Transistor base-to-emitter voltage
V_E	Voltage from emitter to ground
V_{if}	AGC voltage to i-f amplifier
V_{CC}	Collector supply voltage